A Monolithic DC Temperature Compensation Bias Scheme for Multistage HEMT Integrated Circuits

Kevin W. Kobayashi, *Member, IEEE*, William L. Jones, *Member, IEEE*, Keven MacGowan, Richard Kono, and Ling-Shine Jane Lee

Abstract— **This work benchmarks the first demonstration of a multistage monolithic HEMT IC design which incorporates a dc temperature compensated current-mirror bias scheme. This is believed to be the first demonstrated monolithic HEMT bias scheme of its kind. The active bias approach has been applied to a 2–18 GHz five-section low noise HEMT distributed amplifier which achieves a nominal gain of 12.5 dB and a noise figure <2.5 dB across a 2–18 GHz band. The regulated current-mirror scheme achieves better than 0.2% current regulation over a 0–125°C temperature range. The RF gain response was also measured over the same temperature range and showed less than 0.75 dB gain degradation. This results in a −0.006 dB/°C temperature coefficient which is strictly due to HEMT device G_m variation with temperature. The regulated current-mirror circuit can be employed as a stand-alone V_{gs}-voltage reference circuit which can be monolithically applied to the gate bias terminal of existing HEMT IC's for providing temperature compensated performance. This monolithic bias approach provides a practical solution to dc bias regulation and temperature compensation for HEMT MMIC's which can improve the performance, reliability, and cost of integrated microwave assemblies (IMA's) used in space-flight military applications.**

I. Introduction

HEMT TECHNOLOGY is widely used in receiver applications because of its state-of-the-art low noise figure performance at millimeter-wave frequencies. However the nature of the HEMT device structure which is based on critical fabrication techniques such as electron beam lithography for defining sub-0.2 μm gate geometries and molecular beam epitaxy for fabricating a heterostructure, lends itself to variations in device characteristics. A major consequence of the high performance HEMT fabrication technology is the widely varying gate threshold voltages which make HEMT MMIC's difficult to self-bias. Conventional MESFET biasing methods such as resistive feedback and active current source topologies have been applied to HEMT's resulting in as much as ±20% bias current variation which is due to the HEMT's threshold variations with process [1], [2]. For many applications this is inadequate because the HEMT's millimeter wave performance is very sensitive to its bias condition.

In order to bias the HEMT MMIC's, the industry practice is to integrate off-chip regulators in a microwave hybrid assembly. This approach consists of discrete silicon regulators, bypass capacitors, resistors, and several bondwires. Thus, the hybrid approach can be unattractive in terms of size, part count, weight, and reliability. For space qualified applications for instance, these discrete components which can be purchased for a few cents each, may end up costing over ten dollars each to implement as flight qualified hardware after all the reliability and mechanical testing has been performed. An elegant solution is to integrate a *monolithic* regulator with the HEMT MMIC. This would reduce the costs associated with flight or military spec qualification as well as procurement and assembly of the discrete parts.

A previous demonstration of a HEMT current regulator which was monolithically integrated with a single stage LNA achieved ±3% current regulation over ±0.5 V HEMT process threshold variation, and better than 1.5% current regulation over a 25°C–125°C temperature range [3]. For multitransistor circuits which consists of multiple gain stages or functions, a current regulator applied to each HEMT transistor in the circuit becomes unattractive in terms of size and dc power consumption, especially when there may be as many as 5 to 10 HEMT's in a single MMIC. A bias scheme which uses a single current regulator for biasing a multitransistor HEMT IC was also briefly described in [3] but has not been demonstrated.

This work presents the design and measured results of a biasing scheme for multitransistor HEMT IC's which utilize a regulated current-mirror approach. Its practical implementation is demonstrated by integrating the regulated current-mirror with a 2–18 GHz low noise five-section distributed amplifier. For the first time, dc bias regulation and RF performance of the amplifier over temperature will be disclosed. But first, the practical implementation of this dc regulated HEMT monolithic biasing approach will be discussed.

II. Monolithic Regulated Current-Mirror Bias for Multi-Stage HEMT MMIC'S

The monolithic HEMT regulated current-mirror bias scheme is based on a previously demonstrated active bias circuit [3]. In the previous work, a HEMT op-amp was directly integrated with the HEMT device of a single stage LNA to provide dc current regulation, Fig. 1. The HEMT op-amp is used to mirror a voltage reference, V_{ref}, to the drain connection of a current source resistance, R_{load}. A resistive divider

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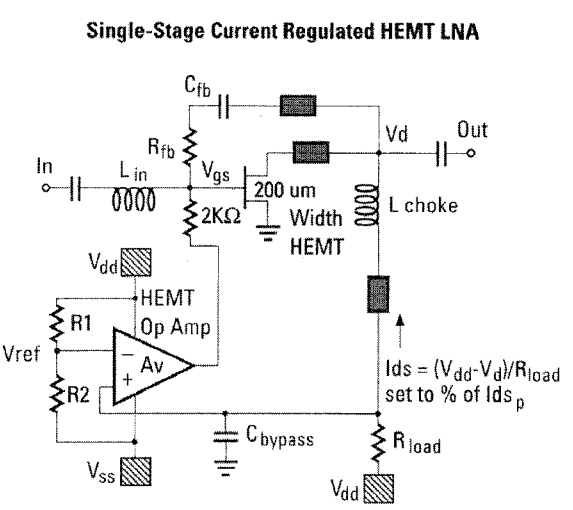

Fig. 1. A HEMT op-amp integrated with the HEMT device of a single stage LNA to provide current regulation.

comprised of resistors R_1 and R_2 is used to set up a voltage reference, $V_{\rm ref}$, which is insensitive to variation in thin-film-resistor (TFR) sheet resistance because it is determined by the ratio of these resistors. The op-amp consists of a high gain HEMT differential amplifier stage with a high differential input impedance, and a source follower output for providing a low impedance output. By using a HEMT op-amp regulator, the bias sensitivity of the amplifier due to process is transferred from the dependence on wafer-to-wafer threshold variations $\Delta V_{\rm gsth_{w-w}}$, which are on the order of ± 0.3–0.5 volts, to the dependence on adjacent device-to-device HEMT threshold match $\Delta V_{\rm gsth_{d-d}}$, which is a few tens of millivolts ($\leq$20 mV). Thus the HEMT op-amp approach provides bias regulation which reduces the HEMT threshold sensitivity by an order of magnitude. This can be illustrated by the following relation given in (1), which expresses the fractional current regulation as a function of HEMT threshold characteristics and design parameters

$$\left[\frac{\Delta I_{\rm ds}}{I_{\rm ds}}\right]_{\Delta V_{\rm gsth}} = -\frac{g_m R_L}{(1+g_m R_L A_v)} \cdot \frac{\Delta V_{\rm gsth}}{[V_{\rm dd}-V_d]} \qquad (1)$$

where g_m and R_L are the regulated HEMT's dc transconductance and load resistor, A_v is the HEMT open-loop op-amp voltage gain, $(V_{\rm dd}-V_d)$ is the voltage drop across the sensing or load resistor of the current source, and $\Delta V_{\rm gsth}$ is the threshold variation due to either process or temperature. The effect of changes in dc threshold, $\Delta V_{\rm gsth}$, due to either process, temperature, or aging, is reduced by the product of the op-amp gain and the dc regulated HEMT gain which is expressed in the first denominator on the left. Thus, the higher the voltage gain of the op-amp A_v, the better the current regulation. The op-amp gain may be expressed as a function of the internal op-amp load resistor $R_{L_{\rm op}}$ and the dc transconductance $G_{m_{\rm op}}$ and source resistance R_s of the HEMT transistors comprising the differential amplifier: $A_v \approx G_{m_{\rm op}} \cdot R_{L_{\rm op}}/(1+G_{m_{\rm op}} \cdot R_s)$. This shows that the op-amp gain can be increased by increasing $R_{L_{\rm op}}$ and/or $G_{m_{\rm op}}$. It also shows that the dc power of the op-amp may be reduced by using smaller gate width HEMT's (at lower $I_{\rm ds}$) and increasing $R_{L_{\rm op}}$. However, there is a limit to using smaller HEMT's and maintaining reliable op-amp performance.

In the regulated current-mirror bias scheme of the present work, we use the same HEMT op-amp scheme to regulate a standard HEMT device which is not part of the RF circuit, depicted in Fig. 2. This "master" or "reference" HEMT device is regulated to a particular bias condition which is expressed as a % of $I_{\rm ds_p}$, where $I_{\rm ds_p}$ is defined as the drain-to-source bias current corresponding to the HEMT's peak transconductance (G_{m_p}). For low noise applications the desired bias current is typically between 25–40% $I_{\rm ds_p}$. The gate-to-source voltage, $V_{\rm gs-ref}$, of the regulated HEMT device is used as a reference which is applied to the HEMT devices in the circuit. The "slave" or circuit HEMT devices in the circuit will bias up to approximately the same % $I_{\rm ds_p}$ as the "master" device which is current regulated. In this manner, a regulated current-mirror bias scheme results which can accommodate several HEMT stages using the same current regulator-voltage reference circuit. The resulting regulator is a portable stand-alone circuit which can be integrated with existing HEMT IC's that require a $V_{\rm gs}$ gate bias.

Although the regulated current-mirror bias scheme described above is simple in concept, several assumptions are made. The first assumption is that for a given $V_{\rm gs}$ voltage, the regulated current bias (% $I_{\rm ds_p}$) will be mirrored between master and slave devices and will be independent of device size. In practice, this is not necessarily the case. Fig. 3 shows the measured % $I_{\rm ds_p}$ of several HEMT device gate widths for different fixed $V_{\rm gs}$ reference voltages. This figure shows that the % $I_{\rm ds_p}$ does not scale perfectly with device width. For a given fixed $V_{\rm gs}$ bias, the % $I_{\rm ds_p}$ decreases as the HEMT device width increases. These figures show that for each of the three different fixed $V_{\rm gs}$ bias conditions, the % $I_{\rm ds_p}$ decreases by $\approx$10% when scaling from a 40 μm to a 200 μm width HEMT. This difference must be taken into account when employing the regulated current-mirror scheme, that is, an adjustment factor must be incorporated based on the device scaling characteristics of the particular HEMT process.

Another assumption which is made when using this current-mirror bias approach is that the regulated "master" HEMT device which is current regulated, has identical dc threshold characteristics as the HEMT devices of the circuit. This difference due to the process variations across the GaAs wafer is dependent on the proximity of the regulated reference device to the circuit devices. These process variations result in threshold mismatches which are typically less than 2–3% in current ($\approx$ 10 mV) for distances less than 1 mm. This is acceptable for most HEMT MMIC applications.

Other factors such as regulation performance sensitivity to adjacent device-device threshold match, $\Delta V_{\rm gsth_{d-d}}$, wafer-to-wafer threshold match, $\Delta V_{\rm gsth_{w-w}}$, supply voltage, and the inherent HEMT op-amp design parameters has already been discussed in detail [3].

Finally, for applications which require multiple bias conditions, i.e., different % $I_{\rm ds_p}$ for different circuit functions, a current regulator for each required bias condition must be integrated. For example, if a HEMT MMIC requires an LNA

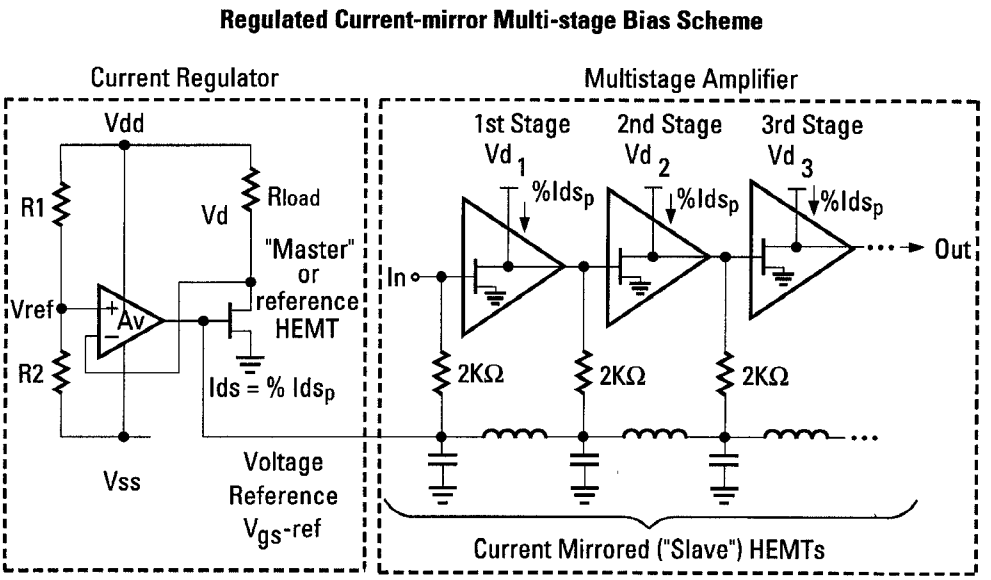

Fig. 2. Regulated current-mirror bias scheme applied to a multistage HEMT IC.

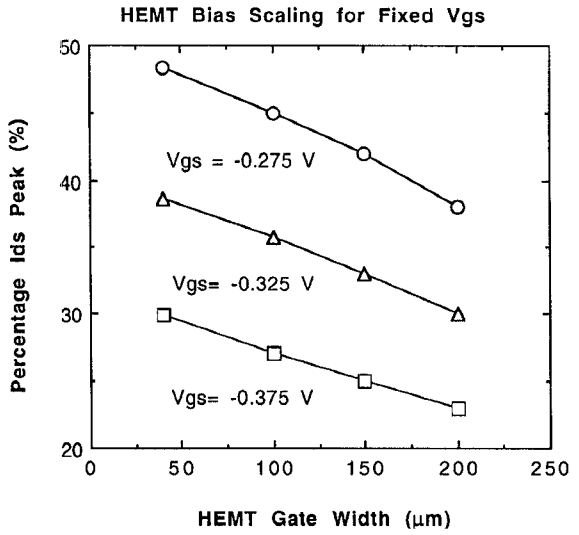

Fig. 3. Measured % I_{ds_p} versus HEMT device gate width for various fixed V_{gs}.

biased at 25% I_{ds_p}, an LO buffer amplifier biased at 50% I_{ds_p}, and an active mixer biased at 70% I_{ds_p}, then the monolithic integration of three separate regulator circuits, one for each bias condition ($\%I_{ds_p}$), would be required. In this situation, the monolithic bias approach is even more desirable since several off-chip regulators and discrete components have been eliminated from the IMA.

III. Application to a 2–18 GHz 5-Stage Low Noise Distributed Amplifier

To demonstrate a practical application of this bias scheme, the regulated current-mirror was integrated with a five-section low noise distributed amplifier. A circuit schematic of the regulated biased HEMT DA is given in Fig. 4. A similar manually biased five-section low noise HEMT DA has been previously reported [4]. The amplifier consists of 90 μm gate width HEMT's for the first and last section, and three 120 μm gate width HEMT's for the intermediate sections of the distributed amplifier. The smaller 90 μm gate width devices were chosen to obtain good input and output return-loss match over the broad band. The bias of each of the 90 μm and 120 μm gate width HEMT's was chosen for low noise figure performance with a 50 Ω source impedance. The optimum bias was determined to be 40% I_{ds_p}, or 58 mA through a total gate width of 0.54 mm. The V_{ds} supply voltage of the HEMT DA is 2.5 V. The HEMT DA was designed for a nominal gain of >10 dB and <2.5 dB noise figure across a 2–18 GHz band.

A current regulator which regulates a 200 μm width HEMT reference device is integrated with the HEMT transistors of the distributed amplifier to form the regulated current mirror biasing scheme. The gate reference voltage of the regulator circuit is applied to the gate voltages of each of the 5 HEMT devices in the amplifier circuit. A standard 200 μm HEMT device was chosen as the reference device. The regulator circuit has provisions for choosing 20%, 30%, and 40% I_{ds_p} bias currents corresponding to 12 mA, 16 mA, and 20 mA I_{ds} through the 200 μm width reference device. Any of these bias conditions can be obtained by applying +7 volts to the respective $V_{d_{ref}}$ pads shown in Fig. 4. Because the mirror devices in the circuit have smaller gate widths than the regulated 200 μm device, the % I_{ds_p} bias of these devices will be larger by ≈7–10% according to Fig. 3. Thus, 30%, 40%, and 50% I_{ds_p} amplifier biases can be obtained, respectively. The regulator circuit requires a +7 V positive supply and a −5 V negative supply. The total nominal current drawn through the regulator circuit is 29 mA including 16 mA from the regulated 200 μm HEMT reference device biased at 30% I_{ds_p}. The regulator can be re-designed with smaller gate

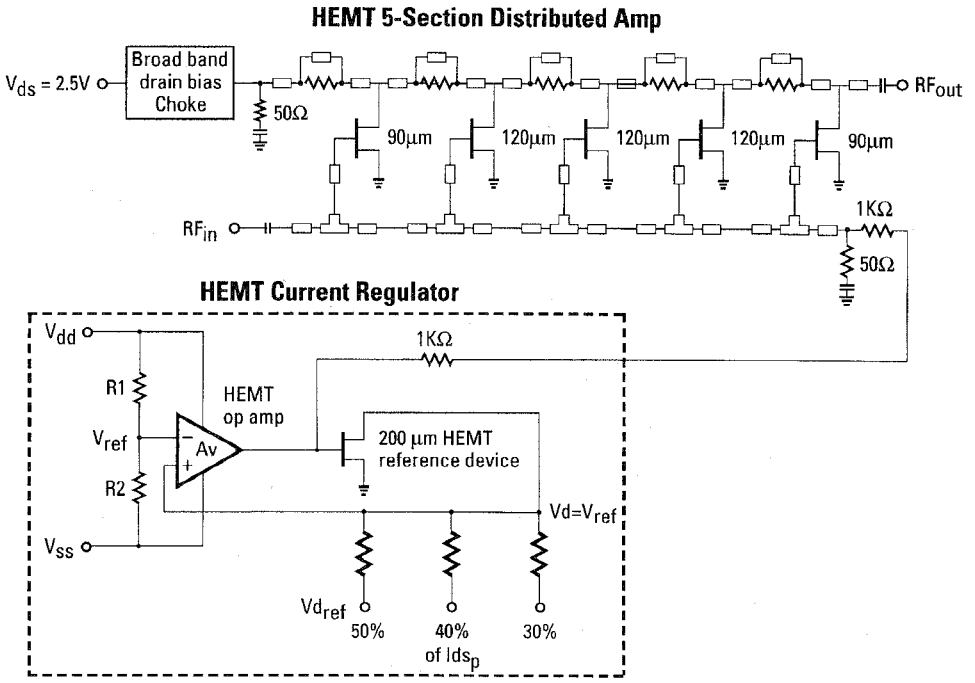

Fig. 4. A circuit schematic of the regulated biased five-section HEMT DA.

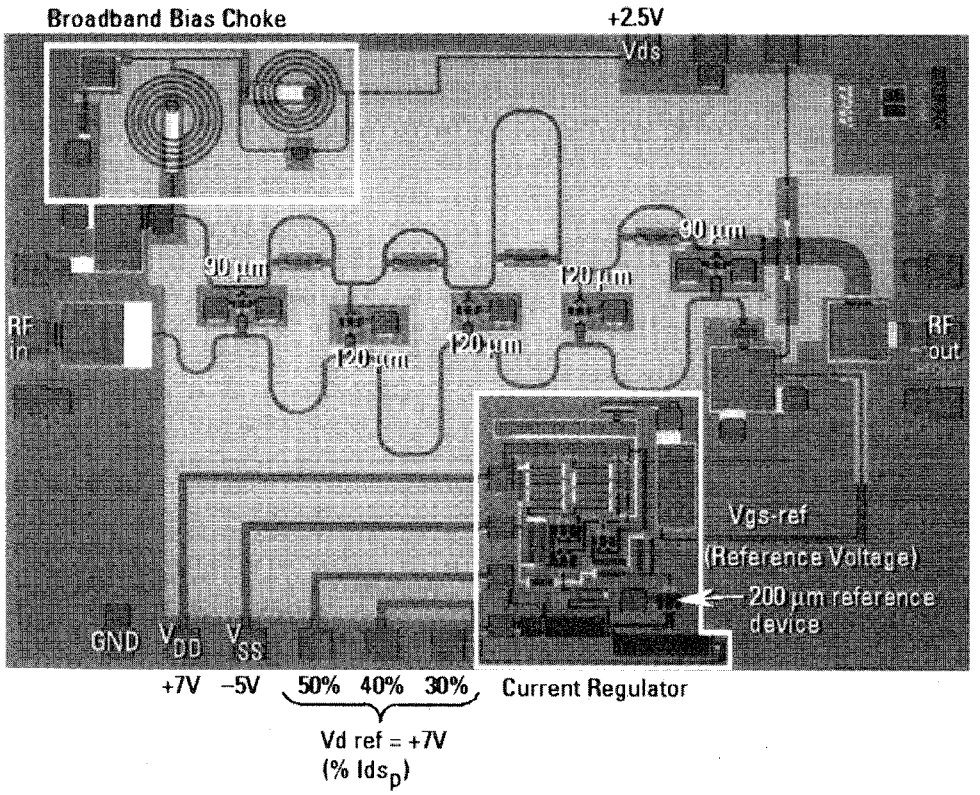

Fig. 5. A photograph of the monolithic regulated HEMT DA.

width devices at the same % I_{ds_p}, in order to reduce the dc power consumed in the regulator circuit. Performance tradeoffs involved in reducing dc bias current and supply voltage of the regulator circuit have been discussed in a previous work [3].

A photograph of the resulting monolithic regulated HEMT DA is shown in Fig. 5. The HEMT DA is biased through a 2.5 V supply on the V_{ds} pad at the top of the chip, and +7 V and −5 V on the V_{dd} and V_{ss} pads located at the bottom of the chip, respectively. A +7 V supply is applied to one

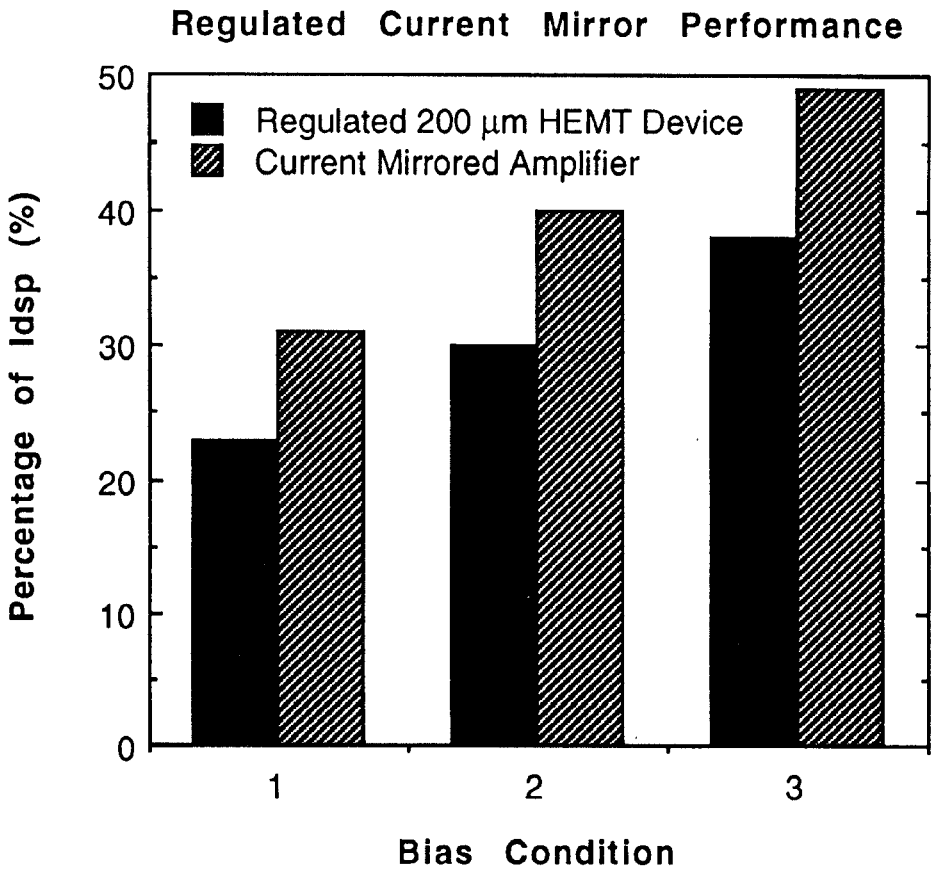

Fig. 6. Dc regulated bias performance of the 200 μm HEMT device and of the five-stage amplifier circuit.

of three $V_{d_{\text{ref}}}$ pads in order to obtain 30, 40, or 50% I_{ds_p} circuit biases. The HEMT current regulator supplies a $V_{\text{gs-ref}}$ voltage to the gate bias feed of the distributed amplifier as illustrated in Fig. 5. Its central location and close proximity to the HEMT devices of the circuit ensure well matched dc threshold characteristics resulting in less than a few percent accuracy. The current regulator fits in a 0.625×0.79 mm^2 area which is only 8% of the total MMIC which is 2.95×2.05 mm^2 in size.

IV. Measured Circuit Performance

The regulated HEMT low noise distributed amplifier was measured for gain, noise figure, and dc current regulation performance. Fig. 6 gives the dc bias performance of the 200 μm reference device and the five-stage amplifier. There are three bias conditions which could be selected corresponding to 23%, 30%, and 38% I_{ds_p} of the 200 μm HEMT reference device. The amplifier circuit which consists of three 120 μm and two 90 μm gate width HEMT's for a total of 0.54 mm of gate periphery, has corresponding biases of 31%, 40%, and 49% I_{ds_p}. This is in agreement with Fig. 3 which shows that there is $\approx$10% increase in bias current (% I_{ds_p}) when mirroring current from the 200 μm reference device to the smaller HEMT devices of the distributed amplifier circuit.

Fig. 7 shows a typical gain and return-loss response of the monolithic regulated five-section low noise distributed amplifier. At a nominal circuit bias of 58 mA which corresponds

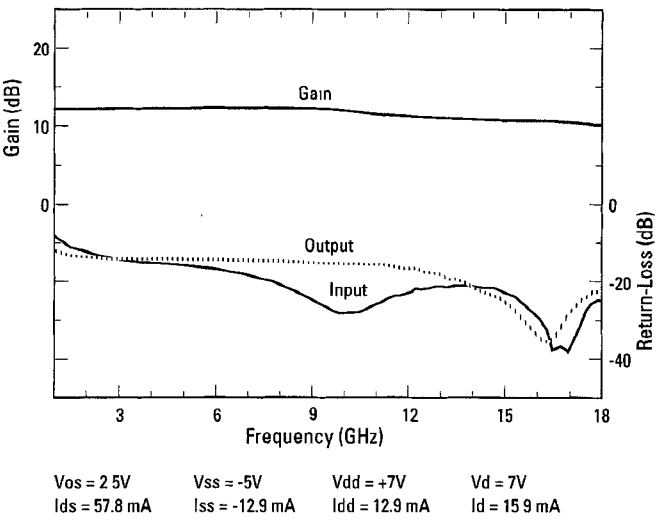

Fig. 7. Typical gain and return-loss response of the five-section low noise distributed amplifier.

to 40% I_{ds_p}, the amplifier achieves <10 dB gain across a 2–18 GHz band, and corresponding input and output return-losses which are better than 12 dB. Typical measured noise figure and IP3 performance at the three different regulated current biases are given in Figs. 8 and 9. The noise figure is typically 2.0 ± 0.25 dB across a 6–18 GHz band and is not sensitive to bias current. The IP3 performance is greater

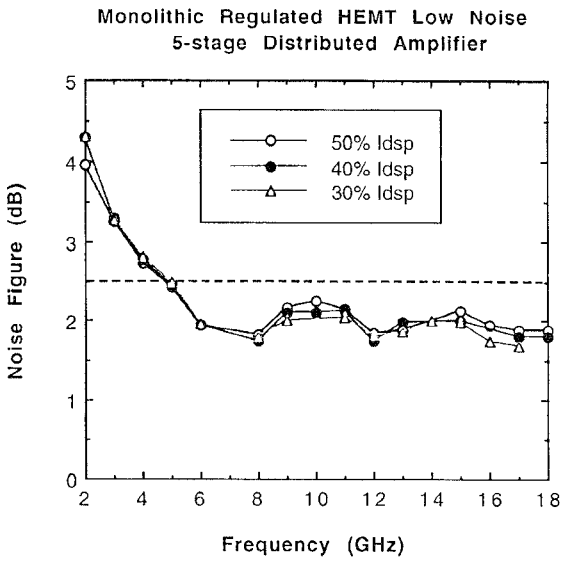

Fig. 8. Typical amplifier wideband noise figure performance for 30%, 40%, and 50% I_{ds_p} current bias.

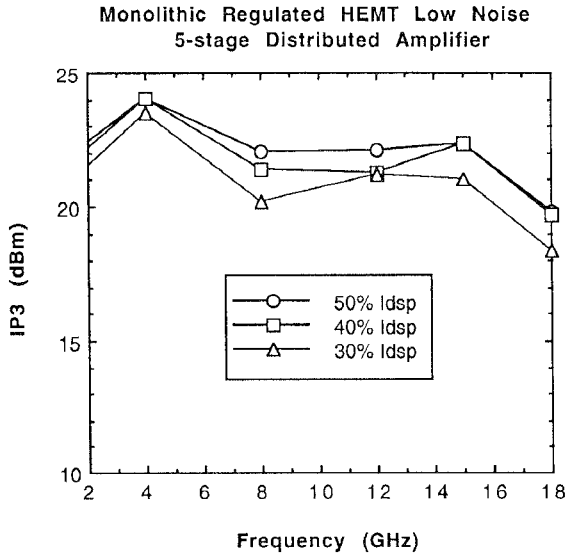

Fig. 9. Typical amplifier wideband IP3 performance for 30%, 40%, and 50% I_{ds_p} current bias

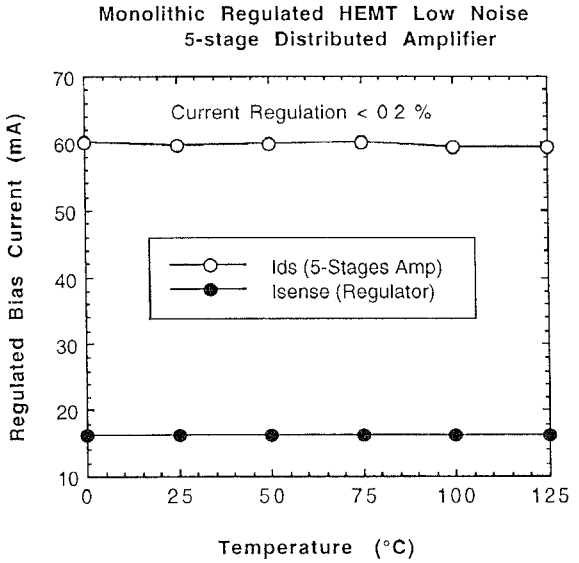

Fig. 10. Dc current regulation performance of the 200 μm HEMT reference device and of the amplifier circuit over temperature.

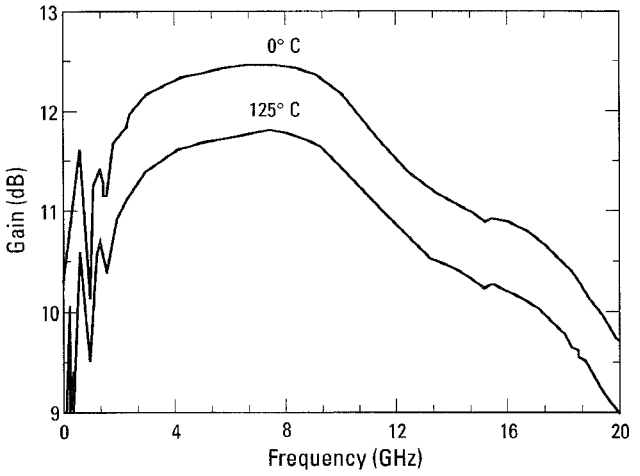

Fig. 11 Wide band gain response of the amplifier taken at 0°C and 125°C

than 20 dBm up to 15 GHz and rolls off by 3 dB at 18 GHz for each of the three bias conditions. As much as a 2.5 dB difference in IP3 can be seen across the three bias conditions. While the noise performance appears to be insensitive to bias, the linearity performance (IP3) of the amplifier seems to be significantly bias dependent. This justifies the need for using a regulated bias scheme which provides a means of maintaining good RF gain and linearity performance of the amplifier by regulating the bias current of the circuit over temperature and HEMT process variations.

The amplifier's dc bias regulation and RF performance were also evaluated on-wafer over temperature. Fig. 10 shows the dc current regulation performance of the 200 μm HEMT reference device and of the amplifier circuit. The 200 μm HEMT was biased at 16 mA or 31% I_{ds_p}, while the amplifier was biased at 58 mA (0.54 mm total gate width) or 40% I_{ds_p}. Both the 200 μm HEMT reference device and the five-stage distributed amplifier were current regulated to within 0.2% over a 0°C–125°C temperature range. Wide band gain responses of the amplifier taken at 0°C and 125°C are shown in Fig. 11. Over the 125°C temperature range, the gain degrades by 0.75 dB. Fig. 12 shows that the gain degrades linearly with increasing temperature. The gain degradation is identical at both 10 GHz and 18 GHz. The gain-temperature coefficient is -0.006 dB/°C. This degradation in gain is strictly due to the intrinsic effect of temperature on the HEMT's transconductance, G_m, independent of bias current. The degradation due to bias current on the HEMT's G_m has been eliminated due to the use of current regulation. This point is further supported by Fig. 13 which gives the measured G_{m_p} (peak transconductance) over temperature of a typical HEMT device. This figure indicates that G_{m_p} degrades by $\approx$10% over a 40°C to 120°C temperature rise. The corresponding calculated gain-

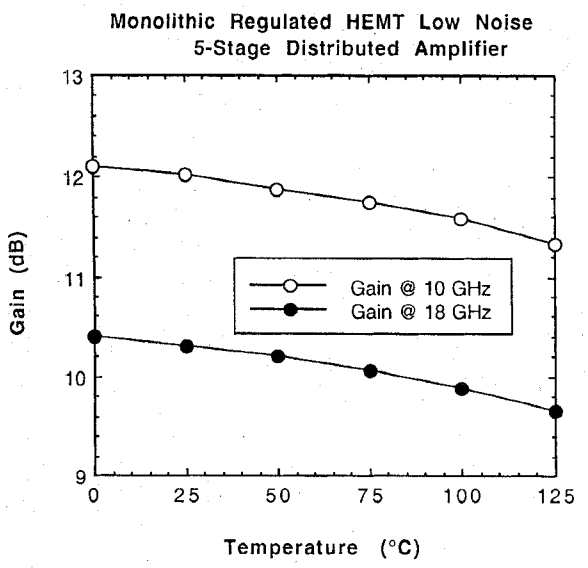

Fig. 12. Gain at 10 GHz and 18 GHz versus temperature.

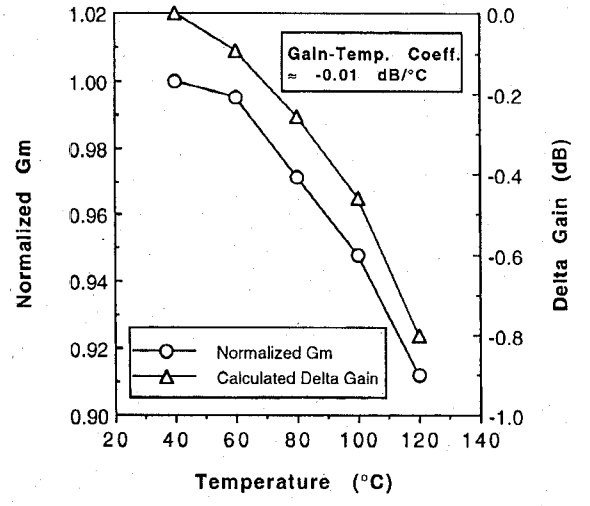

Fig. 13. Measured HEMT device G_{m_p} and calculated device gain degradation versus temperature.

temperature coefficient of the device is ≈ -0.01 dB/°C per stage, and reflects degradation in G_{m_p} which is compounded by the change in bias current, I_{ds_p}, over temperature. The difference between the gain-temperature coefficients of the regulated circuit and the unregulated HEMT device indicates that a significant improvement in RF gain-temperature coefficient is achieved by regulating the bias current.

V. Conclusion

This work describes a novel monolithic HEMT regulated bias scheme which offers a practical solution to HEMT MMIC temperature compensation. A practical application of this bias scheme has been demonstrated with a 2–18 GHz low noise HEMT distributed amplifier. The dc current regulation performance is better than 0.2% over a 0°C–125°C temperature range. The corresponding RF gain degraded by only 0.75 dB over this same temperature range, resulting in a gain-temperature coefficient of -0.006 dB/°C. This is a significant improvement in gain-temperature coefficient when compared to an unregulated HEMT device which achieves a coefficient of -0.01 dB/°C. The monolithic HEMT regulated bias approach provides a practical means of HEMT MMIC self-bias and temperature compensation which is attractive in terms of performance, reliability, and cost of space-flight applications. The authors believe that this development represents a significant step forward in the evolution of HEMT MMIC technology.

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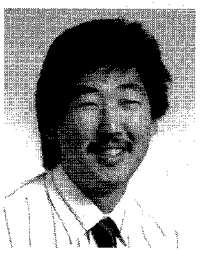

Kevin W. Kobayashi (M'93) was born in San Diego, CA in 1963. He received the B.S.E.E. from the University of California at San Diego in 1986, and the M.S.E.E. degree from the University of Southern California in 1991.

From 1985 to 1986 he worked for Burrough Micro-Components Group in Rancho Bernardo, CA, where he worked on SPICE and two-dimensional device simulation and modeling of LDD MOSFET's. Since 1986 he has been working at TRW's Advanced Microelectronics Laboratory in Redondo Beach, CA, where he has been involved in the development of HBT, HEMT, and MESFET technologies. His primary focus is in the design of HBT and HEMT MMIC's for insertion into TRW systems. He also provides technical design support and instruction for TRW's GaAs HBT commercial foundry service. His research activities have included the development of HBT low phase noise VCO's for synthesizers, the development of broadband techniques for HBT amplifiers, active matching and feedback design development, design topology studies for high linearity VGA's, and the design of low noise receivers and LNA's employing TRW's HBT commercial foundry process for wireless applications. He has also been heavily involved with the development of selective MBE MMIC's which integrate HEMT's, HBT's, PIN's, and high performance Schottky diodes on the same III-V substrate for next generation high performance mixed-mode MMIC applications. He has authored several technical papers on MMIC design and III-V IC technology and has received several patents.

Mr. Kobayashi has been a two-time recipient of the TRW chairman's award for innovation.

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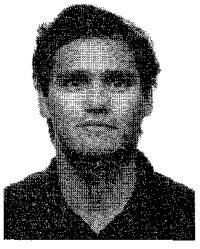
Immediately after graduate school, he joined AT&T Bell Laboratories' Heterojunction IC and Material Department in Murray Hill, NJ, as a Member of the Technical Staff. He was responsible for research and process development of AlGaAs/GaAs heterojunction device fabrication, improvements in ohmic contact formation and reactive ion etching for uniform threshold voltage control. He later joined TRW's Electronic Systems Group in 1985 where he has performed research activities in the area of process development related to the design and fabrication of GaAs heterostructure low noise HEMT microwave devices and MMIC's. He is presently Senior Scientist/Section Manager for the Advanced Technologies Section, responsible for the supervision of research and process development of PIN/HEMT integration, InGaAs and InP MMIC's, and Manager for the HEMT/MESFET Product Section, which is responsible for the transfer and management of HEMT products in TRW's GaAs MMIC Foundry.

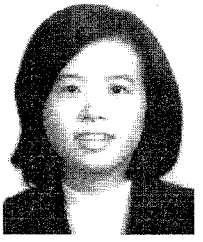


Keven MacGowan received the B.S. degree in electronic engineering from California State University, Long Beach in 1990.

He has been with TRW since 1985. Five years at TRW were spent as a microwave technician and earning the B.S. degree. As a Member of the technical staff, he has been involved in the design of various commercial chips using advanced GaAs technologies. Some of these chips include low noise amplifiers, DRO's and receiver down converters for DBS applications using TRW's GaAs HEMT's.

Richard Kono received the B.S. degree in engineering from the University of California, Los Angeles, in 1979

He has been with TRW since graduation and the GaAs Department since 1986. His primary responsibility is the generation of device models for MESFET, HEMT, and HBT processes.



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She has been a Process Engineer on GaAs IC processing, mostly HEMT MMIC processing, in TRW for over 7 years.